

Group I, Claims 1-4 and 13, drawn to a semiconductor apparatus apparatus and a method thereof is comprised of a data analyzer which comprises a logic circuit and a flip-flop, classified in class 714, subclass 734;

Group II, Claims 5 and 6, drawn to a semiconductor apparatus comprising comparator for comparing input signals, classified in class 714, subclass 719; and

Group III, Claims 7-8, 9-10 and 11-12 and 14, drawn to a semiconductor apparatus and a method thereof for memory testing by comparing memory outputs with expected values, classified in class 714, subclass 718.

It is the Examiner's position that the inventions listed as Groups I, II, and III are distinct from each other.

In response to the Examiner's requirement for restriction, applicant provisionally elects to prosecute the subject matter of Group II, Claims 5 and 6. However, applicant reserves the right under 35 U.S.C. §121 to file one or more divisional applications directed to the non-elected claims in this application.

In view of the foregoing, an examination on the merits of the elected claims, at an early date, is earnestly solicited.

Respectfully submitted,


Paul J. Esatto, Jr.
Reg. No. 30,749

Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343
PJE:ahs